

AMENDMENT TO THE CLAIMS:

Please amend claims 4 and 9-11, without prejudice, and add new claims 12-24, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (original): A stacked-chip semiconductor device comprising:

an interposer substrate; and

a plurality of semiconductor chips overlaid two tiers deep or more and mounted on said interposer chip, wherein

at least one of said semiconductor chips comprises a plurality of through-wires, and at least one voltage selected from power supply voltage and ground is fed from said interposer substrate by way of said through-wires to said at least one of said semiconductor chips.

Claim 2 (original): A stacked-chip semiconductor device comprising:

an interposer substrate;

a first semiconductor chip that is disposed above said interposer substrate and that has a thick-film wiring and a circuit surface on an upper surface;

a second semiconductor chip that is disposed above said first semiconductor chip and that has a plurality of through-wires and a circuit surface on an upper surface;

a plurality of bumps for providing an electrical connection between said plurality of through-wires and said thick-film wiring; and

bonding wires for electrically connecting said interposer substrate and said thick-film wiring, wherein

at least one voltage selected from power supply voltage and ground is fed from said

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interposer substrate to the circuit surface of said second semiconductor chip by way of said bonding wires, said thick-film wiring, said plurality of bumps, and said plurality of through-wires.

Claim 3 (original): A stacked-chip semiconductor device comprising:

an interposer substrate;

a first semiconductor chip that is disposed above said interposer substrate and that has a thick-film wiring and a circuit surface on an upper surface;

a second semiconductor chip that is disposed above said first semiconductor chip and that has a plurality of through-wires and a circuit surface on a lower surface;

a plurality of bumps for providing an electrical connection between said second semiconductor chip and said thick-film wiring; and

bonding wires for electrically connecting said interposer substrate and said thick-film wiring,

wherein a power supply voltage and ground are fed from said interposer substrate to the circuit surface of said second semiconductor chip by way of said bonding wire, said thick-film wiring, and said plurality of bumps; and electrical signals are transmitted between said interposer substrate and the circuit surface of said second semiconductor chip by way of said plurality of through-wires and said bonding wires.

Claim 4 (currently amended): The stacked-chip semiconductor device according to claim 2 ~~claims 2 or 3~~, wherein the thickness of said thick-film wiring is the same as the height of said plurality of bumps.

Claim 5 (original): The stacked-chip semiconductor device according to claim 4, wherein said thick-film wiring and said plurality of bumps are formed by plating.

Claim 6 (original): A stacked-chip semiconductor device comprising:

an interposer substrate;

a first semiconductor chip that is disposed above said interposer substrate and that has a plurality of through-wires;

a second semiconductor chip that is disposed above said first semiconductor chip and that has a circuit surface on a lower surface;

a plurality of first bumps for electrically connecting said plurality of through-wires and said interposer substrate; and

a plurality of second bumps for electrically connecting said plurality of through-wires and said second semiconductor chip,

wherein at least one voltage selected from power supply voltage and ground is fed from said interposer substrate to the circuit surface of said second semiconductor chip by way of said first bumps, said thick-film wiring, and said second bumps.

Claim 7 (original): A stacked-chip semiconductor device comprising:

an interposer substrate;

a first semiconductor chip that is disposed above said interposer substrate and that has a circuit surface on an upper surface and a thick-film wiring;

a spacer that is disposed above said first semiconductor chip and that has a plurality of through-wires;

a second semiconductor chip that is disposed above said spacer and that has a circuit surface on a lower surface;

a plurality of first bumps for electrically connecting said plurality of through-wires and said thick-film wiring;

a plurality of second bumps for electrically connecting said plurality of through-wires and said second semiconductor chip; and

bonding wires for electrically connecting said interposer substrate and said thick-film wiring,

wherein at least one voltage selected from power supply voltage and ground is fed from said interposer substrate to the circuit surface of said second semiconductor chip by way of said bonding wires, said thick-film wiring, said first bumps, said plurality of through-wires, and said second bumps.

Claim 8 (original): A stacked-chip semiconductor device comprising:

an interposer substrate;

a first semiconductor chip that is disposed above said interposer substrate and that has a plurality of first through-wires;

a spacer that is disposed above said first semiconductor chip and that has a plurality of second through-wires;

a second semiconductor chip that is disposed above said spacer and that has a circuit surface on a lower surface;

a plurality of first bumps for electrically connecting said interposer substrate and said first through-wires;

a plurality of second bumps for electrically connecting said first through-wires and said second through-wires; and

a plurality of third bumps for electrically connecting said second through-wires and second semiconductor chip,

wherein at least one voltage selected from power supply voltage and ground is fed from

said interposer substrate to the circuit surface of said second semiconductor chip by way of said first bumps, said first through-wires, said second bumps, said second through-wires, and said third bumps.

Claim 9 (currently amended): A stacked-chip semiconductor device comprising:

an interposer substrate;

a first semiconductor chip that is disposed above said interposer substrate and that has a circuit surface on an upper surface and thick-film wiring;

a second semiconductor chip that is disposed above said first semiconductor chip and that has a plurality of through-wires;

a third semiconductor chip that is disposed above said second semiconductor chip and that has a circuit surface on a lower surface;

a plurality of first bumps for electrically connecting said plurality of through-wires and said thick-film wiring;

a plurality of second bumps for electrically connecting said plurality of through-wires and said second semiconductor chip ~~[[2]]~~; and

bonding wires for electrically connecting said interposer substrate and said thick-film wiring,

wherein at least one voltage selected from power supply voltage and ground is fed from said interposer substrate to the circuit surface of said third semiconductor chip by way of said bonding wires, said thick-film wiring, said first bumps, said plurality of through-wires, and said second bumps.

Claim 10 (currently amended): The stacked-chip semiconductor device according to claim 1 ~~any of claims 1 to 9~~, wherein a plurality of wires for each said semiconductor chip for feeding

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said power supply voltage and ground are disposed in parallel for each said semiconductor chip, and are each connected in parallel to a single wire within said interposer substrate, within said semiconductor chip, or within said spacer.

Claim 11 (currently amended): The stacked-chip semiconductor device according to claim 1 ~~any of claims 1, 2, and 6 to 9~~, wherein a signal is also transmitted, in addition to at least one said power supply voltage and ground, by way of said through-wires.

Claim 12 (new): The stacked-chip semiconductor device according to claim 3, wherein the thickness of said thick-film wiring is the same as the height of said plurality of bumps.

Claim 13 (new): The stacked-chip semiconductor device according to claim 12, wherein said thick-film wiring and said plurality of bumps are formed by plating.

Claim 14 (new): The stacked-chip semiconductor device according to claim 2, wherein a plurality of wires for each said semiconductor chip for feeding said power supply voltage and ground are disposed in parallel for each said semiconductor chip, and are each connected in parallel to a single wire within said interposer substrate, within said semiconductor chip, or within said spacer.

Claim 15 (new): The stacked-chip semiconductor device according to claim 3, wherein a plurality of wires for each said semiconductor chip for feeding said power supply voltage and ground are disposed in parallel for each said semiconductor chip, and are each connected in parallel to a single wire within said interposer substrate, within said semiconductor chip, or within said spacer.

Claim 16 (new): The stacked-chip semiconductor device according to claim 6, wherein a plurality of wires for each said semiconductor chip for feeding said power supply voltage and ground are disposed in parallel for each said semiconductor chip, and are each connected in

parallel to a single wire within said interposer substrate, within said semiconductor chip, or within said spacer.

Claim 17 (new): The stacked-chip semiconductor device according to claim 7, wherein a plurality of wires for each said semiconductor chip for feeding said power supply voltage and ground are disposed in parallel for each said semiconductor chip, and are each connected in parallel to a single wire within said interposer substrate, within said semiconductor chip, or within said spacer.

Claim 18 (new): The stacked-chip semiconductor device according to claim 8, wherein a plurality of wires for each said semiconductor chip for feeding said power supply voltage and ground are disposed in parallel for each said semiconductor chip, and are each connected in parallel to a single wire within said interposer substrate, within said semiconductor chip, or within said spacer.

Claim 19 (new): The stacked-chip semiconductor device according to claim 9, wherein a plurality of wires for each said semiconductor chip for feeding said power supply voltage and ground are disposed in parallel for each said semiconductor chip, and are each connected in parallel to a single wire within said interposer substrate, within said semiconductor chip, or within said spacer.

Claim 20 (new): The stacked-chip semiconductor device according to claim 2, wherein a signal is also transmitted, in addition to at least one said power supply voltage and ground, by way of said through-wires.

Claim 21 (new): The stacked-chip semiconductor device according to claim 6, wherein a signal is also transmitted, in addition to at least one said power supply voltage and ground, by way of said through-wires.

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Claim 22 (new): The stacked-chip semiconductor device according to claim 7, wherein a signal is also transmitted, in addition to at least one said power supply voltage and ground, by way of said through-wires.

Claim 23 (new): The stacked-chip semiconductor device according to claim 8, wherein a signal is also transmitted, in addition to at least one said power supply voltage and ground, by way of said through-wires.

Claim 24 (new): The stacked-chip semiconductor device according to claim 9, wherein a signal is also transmitted, in addition to at least one said power supply voltage and ground, by way of said through-wires.

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